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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LE, DINH THANH	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/733,605	GARY JOHNSON	
	Examiner	Art Unit	
	DINH T. LE	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2005*.

2a)☒ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 25-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 25-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections

Claim Rejections - 35 USC § 112

Claims 1-10 and 25-44 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction or clarification is required.

In claim 1, it is unclear what the "feedback signal" is, where "feedback signal" and "capacitive delay" come from, how the delay circuit can switch an activation of the capacitance delay since no means for perform the switching function is recited in the claim. The same is true for claims 25 and 35.

In claim 4, the recitation "said coarse delay" on line 2 lacks clear antecedent basis. The description of the present invention is complete because the "coarse delay", "fine delay" and "phase detector" are not connected to anything. Thus, the claimed delay locked loop may not perform the recited function. Also, it is unclear how the phase detector can "recognize" said phase difference on line 6. The same is true for claims 28 and 37.

In claim 5, the description of the present invention is incomplete because the "first inverter", transistors" and a "second inverter" are not connected to anything. Thus, they may not

perform the recited function. It is not understood how the second inverter can provide "complementary control signal" since the inverter is only the means for inverting a signal, and how the recitation "first and second inverters", "N-channel transistor set" and "P-channel transistor set" as combined is read on the preferred embodiment. Insofar as understood, no such transistors and inverters are seen on the drawings. . The same is true for claims 29 and 39.

In claim 6, the recitation "said input delay" on line 2 lacks clear antecedent basis and "capacitive delay" on line 2 is confusing because it is unclear if this is additional "capacitive delay" or further recitation of previously claimed "capacitive delay" on line 4 of claim 1. It is not clear where the input delay comes from. The same is true for claims 7, 30-31 and 40-41.

In claim 8, it is unclear how the recitation "N-channel transistor sets" and "P-channel transistor sets" is read on the preferred embodiment. Insofar as understood, no such sets are seen on the drawings. The description is incomplete because the claimed transistor sets are not connected to anything. Thus, the claimed sets may not perform the recited function. The same is true for claim 32 and 42.

In claim 9, the recitation "said coarse delay" and "said fine delay" lacks clear antecedent basis. It is not understood how the output signal can have a coarse delay and fine delay and where they come from. The same is true for claims 33 and 43.

In claim 25, it is unclear what the "memory location" on line 2 is, how the location can store data since the location is a place which can not store the data. The recitation "data" on line 7 is confusing because it is unclear if this is additional "data" or further recitation of the previously claimed "data" on line 2.

The remaining claims are dependent from the above claims and therefore also considered indefinite.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 9-10, 35-38 and 43-44 are rejected under 35 USC 102 (b) as being anticipated by Bhullar et al (US 6,327,318).

Bhullar et al discloses in Figures 1-2 a DLL circuit comprising:

- a coarse delay circuit (13);
- a fine delay circuit (15);
- a phase detector (1),
- a feedback signal (FLCK) generated by a delay means (23);

wherein the DLL circuit is used as a signal source for a memory device such as SRAMS, see line 59-67, column 1; and

wherein the delay circuit comprising inverters (17), capacitors (21) and a switch (11), see Figure 2, for switching an activation using the switch (11).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5-8 and 39-42 are rejected under 35 USC 103 (a) as being unpatentable over Bhullar et al (US 6,327,318) in view of Fujii et al (US 6,700,434).

Bhullar et al discloses in Figures 1-2 a DLL circuit comprising all of the limitations of the claimed invention as stated above but does not disclose that the delay circuit comprising inverters, a N-channel transistor set and P-channel transistor sets as recited in the claims.

Fujii etal suggests in Figure 12 a switchable delay circuit comprising delay blocks, each blcok having switches (Sn1-Snn, Sp1-Spn), N-channel transistor set (Can1-Cann) and P-channel transistor set (Cap1-Capn) for increasing delay amount of the delay blocks, see lines 30-34, column 13.

It would have been obvious to a person having skill in the art at the time the invention was made to employ the delay blocks suggested by Fujii et al in the delay circuit of Bhullar et al for the purpose of increasing the delay amount for the delay blocks.

Claims 25-34 are rejected under 35 USC 103 (a) as being unpatentable over Shieh et al (US 6,323,705) in view of Bhullar et al (US 6,327,318) and further in view of Fujii et al (US 6,700,434).

Shieh et al discloses in Figure 1 a circuit comprising:

- a memory (DRAM 13) for storing data;
- a DLL (11); and
- a second device (12) coupled to the memory (13) for access data based on the operation performed by the DLL (11).

However, Shieh et al does not disclose that the DLL comprising a delay circuit for switching an activation of a capacitive delay as recited in claim 25 and the delay blocks having sets of a N-channel transistors and P-channel transistors as recited in claim 29.

Buhllar et al suggests a DLL circuit in Figures 1-2 as stated above with the delay ciruit (111, 17, 21) for compensating for tracking differences between switchable coarse and fine delay, see lines 48-59, column 2.

Fujii etal suggests in Figure 12 a switchable delay circuit comprising delay blocks, each having switches (Sn1-Snn, Sp1-Spn), N-channel transistor set (Can1-Cann) and P-channel transistor set (Cap1-Capn) having the drains and sources being coupled together for increasing delay amount of the delay blocks, see lines 30-34, column 13.

It would have been obvious to a person having skill in the art at the time the invention was made to employ the DLL circuit suggested by Bhuhllar et al and the delay blocks as suggested by Fujii et al in the circuit of Shieh et al for the purpose of compensating for tracking differences

between switchable coarse and fine delay elements, and increasing the delay amount for the delay blocks.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DINH T. LE whose telephone number is (571) 272-1745. The examiner can normally be reached on Monday-Friday (8AM-7PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY CALLAHAN can be reached at (571) 272-1740.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DINH LE
Primary Examiner